REMARKS/ARGUMENTS

Claims 1-9 and 11-15 are pending in this application. Claims 1-9 and 11-15 stand rejected. In particular, claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by Ichikawa U.S. Patent No. 6,285,235. Furthermore, claims 1-6 and 8 stand rejected under 35 U.S.C. §103 as being unpatentable over Junge DE 28 31 495 in view of Klausecker DE 3,202,319.

Before addressing the rejections, Applicants apologize for submitting an incomplete reference DE 3202319 with the IDS submitted July 14, 2005. Apparently, some of the pages were missing including the drawings. A new Information Disclosure Statement with the Reference DE 32 02 319 is submitted herewith.

Turning now to the rejection, the Examiner first rejects claim 1 under 35 U.S.C. §102(b) as being anticipated by Ichikawa U.S. Patent No. 6,285,235.

The Examiner first refers to Fig. 23 of Ichikawa. This figure shows a power switching transistor 1 and a dv/dt detecting circuit 20. The Examiner then refers to Fig. 19 of Ichikawa which shows a capacitor 6A. The Examiner states that a first terminal of the storage capacitor 6A is coupled to a first main electrode while a second terminal of the storage capacitor is coupled to a reference voltage comprising the negative terminal of the voltage source 2B in Fig. 19. The Examiner then refers to Fig. 21 and combines the sensing circuit of Fig. 23 comprising reference items 20, 21 and 22 and 3E in Fig. 23 and reference items 15, 17, 18 and 3E in Fig. 21. The Examiner asserts that these circuits show a protection switch for sensing the rate of change of voltage dv/dt by the block 20 in Fig. 23 with respect to time at the first main electrode of the power switching transistor. The Examiner asserts that the sensing circuit senses the rate of change of the voltage between the main electrodes, i.e., the main electrode E in Fig. 23 with respect to another electrode C in Fig. 23. The Examiner then refers to the rate of change being proportional to the magnitude of the current flowing through the main electrode since the transistor current at least partially flows through the capacitor 6A in Fig. 19, and the Examiner refers to the well-known equation that $I = cdv/dt$ in a capacitor.

First of all, the Examiner refers to a number of mutually inconsistent circuits in the Ichikawa reference. The circuits of Fig. 19, 21 and 23 all show different gate control

circuits. The circuit of Fig. 19 shows a capacitor 6A connected to the emitter of the power switch 1. However, this capacitor is not shown in Figs. 21 and 23 because it is not used in those circuits. A person of skill in the art would not combine these mutually inconsistent circuits, each of which sense a different parameter.

The capacitor 6A is not shown in Figs 21 and 23 because it is not used in those circuits and there is no teaching, suggestion or motivation to combine the embodiment of Fig 19 with the embodiment of Fig 23 of Ichikawa. In a recent Court of Appeals case, Net MoneyIn Inc. v. VeriSign Inc. decided on Oct 20, 2008, it was decided that a prior art reference, in order to anticipate under 35 U.S.C. 102, must not only disclose all the elements of a claim, but must also disclose those elements "arranged as in the claim." Clearly, Ichikawa does not disclose the elements of claim 1 arranged as claimed.

In addition, Ichikawa is silent as to the function and purpose of capacitor 6A with respect to the embodiment shown in Figure 19. Ichikawa offers the most discussion as to the function of capacitor 6A in the description of the embodiment shown in Figure 18. Ichikawa explains that the stray capacitance 14 of the IGBT 1 (power switching transistor) is transferred to capacitor 6A. Ichikawa also states that if IGBT 1 fails and short circuits, then transistor 23 B is protected by capacitor 6A and resistor 4 A. (See Col 9, lines 6-18.) The capacitor of claim 1 in the present application is used as a storage capacitor, and it is NOT used to protect other circuit elements as taught by Ichikawa. Additionally, Ichikawa's capacitor 6A does not even protect the power switching device, IGBT 1. Instead, it is protects a different transistor in the event that IGBT1 fails.

Furthermore, turning to the circuit of Fig. 19, if the transistor 23A turns on, the gate current flows via gate resistor 4 to the IGBT. If transistor 23B is turned on, off gate current IG flows via the gate resistor 4. There is no teaching or suggestion in Fig. 19 of a sensing circuit that senses the rate of change of voltage with respect to time across a storage capacitor wherein the rate of change of voltage is proportional to the magnitude of the current flowing through the power switching transistor. Fig. 19 does not show any sensing circuit for sensing the rate of change of voltage across the storage capacitor.

The Examiner then refers to Fig. 21 but Fig. 21 does not supply any missing teaching. Fig. 21 shows a current sensor 15 but there is nothing to suggest that the current sensor senses the rate of change of voltage across a storage capacitor at the main

terminal of the IGBT1. In fact, the current sensor directly senses the current through the IGBT1, not the rate of change of voltage across a storage capacitor connected in series with the switch. Fig. 21 does not show a capacitor connected in series with the IGBT, but there is no suggestion that a capacitor like the capacitor 6A in Fig. 19, should be connected to be in series with the switch 1. Further, it is precisely so as to eliminate the series current sensor (to reduce voltage drops or an expensive current transformer) that the present invention uses sensed dv/dt at the main terminal of the switch (across the series connected capacitor) to indirectly determine the current through the switch (because with a series capacitor, the current in the capacitor is substantially the current through the switch).

The Examiner then refers to Fig. 23 which does shows a dv/dt detecting circuit. However, as the Examiner concedes, that dv/dt detecting circuit is coupled across the switching transistor 1, that is, between the emitter and collector. Accordingly, the dv/dt detecting circuit 20 of Fig. 23 detects the rate of change of voltage with time across the switching transistor 1. In contrast, the present invention uses a series circuit comprising the power switching transistor and the storage capacitor and a sensing circuit which senses the rate of change of voltage with respect to time across the storage capacitor in series with the power switching transistor wherein the rate of change of voltage is proportional to the magnitude of the current flowing through the power switching transistor. There is no capacitor shown in the circuit of Fig. 23 and there is no teaching or suggestion that such a capacitor should be placed in series with the first and second main electrodes of the power switch 1. Accordingly, there is no teaching or suggestion that the dv/dt detecting circuit detects the rate of change of voltage with respect to time across the storage capacitor wherein the rate of change of voltage is proportional to the magnitude of the current flowing through the power switching transistor.

Because, there is no suggestion that a capacitor such as the capacitor 6A of Fig. 19 should be added to the circuit of Fig. 23, there is, accordingly, no teaching or suggestion of the invention recited in claim 1.

The Examiner then rejects claims 1-6 and 8 under 35 U.S.C. §103 as being unpatentable over Junge in view of Klausecker.

The Examiner first refers to the Junge reference. Junge shows a switch T coupled in series with a capacitor Cd across a DC bus coupled to an inverter WR. The Examiner admits that Junge does not disclose the control circuit for controlling the power switch.

Regarding the Junge reference, the Examiner stated that Junge discloses a power switching transistor (T in Fig. 1) where the first main electrode is coupled to a capacitor. The Examiner further states that the power switching transistor is used to protect the capacitor, and then the Examiner concludes that Junge discloses the problem of protection of storage capacitors against surges and the method of protection by switching the power transistor. The present invention as recited in claim 1 is directed towards protecting the power switching transistor and not the capacitor as taught by Junge. Additionally, the power switching transistor itself of claim 1 does not provide any means of protection. Rather the sensing circuit, in particular, the protection switch, protects the power switching transistor. The Examiner may have misunderstood the separate functions of the power switching transistor and the protection switch, and further misunderstood the problem that the invention solves, namely protecting the power switching transistor, and not a capacitor.

The Examiner then refers to Klausecker and in particular, Fig. 5 of Klausecker. The Examiner reasons that the capacitor C coupled in series with the Resistor R and a zener diode Z across the drain source terminals of the switch LT comprises a sensor circuit for detecting the rate of change dv/dt. The Examiner reasons that because the capacitor is coupled to a fixed potential through the diode Z that the voltage across the capacitor depends exclusively on the drain voltage of the power transistor and that therefore the circuit senses dv/dt.

Applicants direct the Examiner's attention to the claims. Claim 1 states that the sensing circuit senses the rate of change of voltage with respect to time across the series connected storage capacitor wherein <u>the rate of change of voltage is proportional to the magnitude of the current flowing through the power switching transistor</u>.

Applicant refers to the circuit diagram of the present invention. The storage capacitor C4 is in series with the switch Q1. As a result, the current through the capacitor C4 is equal to Cdv/dt, as the Examiner recognizes. This is also primarily the current flowing the transistor Q1 because the capacitor C4 is in series with the switch Q1.

Accordingly, because the top terminal of capacitor C4 is connected to the first main terminal of the transistor Q1, the current through the first main terminal of Q1 is equal to the rate of change of voltage (across the capacitor) at the first main terminal. This is because current I through the capacitor C4 = C/dv/dt.

The Klausecker reference does not teach or suggest this arrangement. Capacitor C of Klausecker is essentially coupled in parallel to the drain source path of the transistor LT. The current through the capacitor and the current through the drain source path of the transistor LT are arranged in a current divider. The current through the capacitor C is thus not the current through the switch LT or the current through one of the main terminals of the switch LT. The current in the capacitor C, because it is essentially in parallel to the switch LT, is proportional to the rate of change of voltage across the switch LT (essentially the rate of change of voltage across the capacitor C), not the magnitude of the current flowing through the switch.

Thus, Klausecker's circuit senses dv/dt <u>across</u> the switch, not dv/dt across a storage capacitor that is proportional to the <u>magnitude of the current flowing through the power switching transistor</u>.

This is because the capacitor C is not disposed in series with the drain source path of the transistor LT but in parallel with it. In fact, the current through the capacitor C in Fig. 5 of Klausecker is proportional to the dv/dt across the switch LT much like the circuit of Fig. 23 of Ichikawa. However, that rate of change of voltage is not proportional to the magnitude of the current flowing through the power switching transistor because the capacitor C is connected in parallel to the switch LT and not in series with it.

In order to better define the invention, the independent claims have been amended to recite that the storage capacitor is coupled in series with the first and second main electrodes of the power switch, and that the rate of change of voltage with respect to time is sensed <u>across the storage capacitor</u> wherein the rate of change of voltage is proportional to the magnitude of the current flowing through the power switching transistor.

Accordingly, Applicants submit that the claims are not taught or suggested by the combination of Junge and Klausecker.

With respect to the remaining claims, the Examiner has also cited the Ohura et al. reference U.S. Patent No. 5,818,281. However, Ohura et al. does not rectify the deficiencies of the Junge and Klausecker references and accordingly fails to teach or suggest the invention.

In view of the above, Applicants request reconsideration and submit that all claims in this application are now in condition for allowance, prompt notification of which is requested.

A Notice of Appeal has also been filed concurrently herewith.

Respectfully submitted,

THIS CORRESPONDENCE IS BEING SUBMITTED ELECTRONICALLY THROUGH THE PATENT AND TRADEMARK OFFICE EFS FILING SYSTEM ON DECEMBER 17, 2008

Louis C. Dujmich
Registration No.: 30,625
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

LCD/jh